CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. - 18. (Canceled)

19. (Currently Amended) A system comprising:

a data processor having:

an input/output buffer; and

cache memory to store data associated with a memory device;

a bus interface unit having a first input/output buffer coupled to the input/output buffer of the data processor, a second input/output buffer and a third input/output buffer, said bus interface unit to:

determine a validity of data in said cache memory during a cache access; and

provide a notification indicating data in said cache memory is valid, wherein said notification identifies a first request;

said memory device having an input/output buffer coupled~~,~~ to said memory device to provide data associated with a first request;

a bus controller having a first input/output buffer coupled to the input/output buffer of the data processor, a second input/output buffer coupled to the second input/output buffer of the bus interface unit and a third input/output buffer, said bus controller to:

receive said first request to access data in said memory device, wherein said first request is received from a bus client;

provide said first request to the memory controller;

receive said data associated with said first request from said bus interface unit;

the memory controller having a first input/output buffer coupled to the third input/output buffer of the bus controller, a second input/output buffer coupled to the third input/output buffer of the bus interface unit and a third

input/output buffer coupled to the input/output buffer of the memory device, said memory controller to:

provide access to said memory device;

receive said first request from said bus controller;

prepare said first request to access data from said memory device;

provide a second request to said bus interface unit, wherein said second request is to access data associated with said first request from said cache memory;

receive said notification from said bus interface unit;

generate a second identifier using said notification;

store said second identifier as part of a kill list, wherein said kill list identifies requests to be terminated; and

terminate the first request based on the kill list.

20. (Previously Presented) The system as in Claim 19, wherein said bus interface unit is further used to synchronize said cache memory to said memory device.

21. (Previously Presented) The system as in Claim 20, wherein said bus interface unit is further used to determine a coherency between said cache memory and said memory device.

22. (Previously Presented) The system as in Claim 21, wherein the coherency is dependent on whether said memory device has been written to prior to a synchronization of said cache memory with said memory device.

23. (Original) The system as in Claim 19, wherein said bus controller includes a peripheral component interconnect bus controller.

24. (Original) The system as in Claim 19, wherein said memory device includes random access memory.

25. (Previously Presented) The system as in Claim 19, wherein said memory controller is further used to:

assign a first identifier to said first request; and

identify said first request from a plurality of pending requests using said first identifier.

26. (Canceled)

27. (Previously Presented) The system as in Claim 19, wherein said memory controller to terminate the first request is further to discard data received from said memory device, wherein said data is associated with said first request.

28. (Canceled)